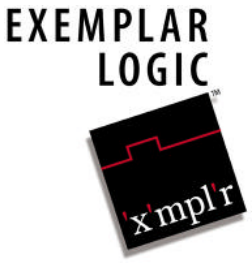

Public Training

Dates: Public training classes are held the first week of every month in San Jose. To find out about the next course, call 800-632-3742 or send an email to sales@exemplar.com.

Galileo Course Objective

The aim of the course is to educate the attendee regarding the use of a Hardware Description Language (HDL) -- VHDL or Verilog HDL -- for design entry and synthesis.

Galileo Abstract

This two-day course is focused on the use of HDLs for synthesis. Each course focuses on a single HDL, either VHDL or Verilog HDL. Course topics and materials focus on using real circuits, such as state machines, to educate the engineer. Hands-on training is an integral component of the seminar, with most design exercises using FPGAs as the target technology.

The first morning covers the use of the Galileo Logic Explorer tool. Different applications Galileo Logic Explorer are discussed, including high-level design with HDLs, hierarchical design entry, and migration and retargeting. The techniques and design flows for satisfying these applications are presented using real design examples. Also presented is the architecture-specific optimization technology Galileo Logic Explorer employs, including algorithms for random logic and module generation for data path logic. The remainder of the day is devoted to learning language basics for the specific HDL being covered, including beginning circuit design.

The second day of the course focuses on the use of the HDL for circuit design, and synthesis-specific issues related to the use of HDLs for design. (One section is called Tricks and Traps, and helps the user to focus on understading what will result from synthesizing various HDL constructs.) More advanced topics, such as the use of hierarchy and timing analysis (and constraints) are also covered. Differences between simulatable and synthesizable HDL code are discussed. The high-level design methodology is discussed in more detail.

Tool

The software used is Exemplar's Galileo Logic Explorer synthesis software. Galileo Logic Explorer is a vendor-independent FPGA synthesis tool that uses architecuture-specific synthesis algorithms to permit designers to fully utilize the target devices. Inputs to Galileo Logic Explorer include VHDL, Verilog HDL, FPGA netlists, and EDIF 200 netlists.

Outputs are gate-level netlists, ready for place and route, and other netlist formats for simulation and schematic generation. Technologies supported include Actel, Altera, AMD, Crosspoint, Cypress, Lattice, Lucent Technology, Motorola, QuickLogic and Xilinx FPGAs and CPLDs.

Leonardo Course Objective

The aim of the course is to educate the attendee regarding the use of a Hardware Description Language (HDL) -- VHDL or Verilog HDL -- for design entry and synthesis.

Leonardo Abstract

This two-day course is focused on the use of HDLs for synthesis. Each course focuses on a single HDL, either VHDL or Verilog HDL. Course topics and materials focus on using real circuits, such as state machines, to educate the engineer. Hands-on training is an integral component of the seminar, with most design exercises using FPGAs as the target technology.

The first morning covers the use of Exemplar Logic's Leonardo synthesis. Different applications Leonardo are discussed, including high-level design with HDLs, hierarchical design entry, and migration and retargeting. The techniques and design flows for satisfying these applications are presented using real design examples. Also presented is the architecture-specific optimization technology Leonardo employs, including algorithms for random logic and module generation for data path logic. The remainder of the day is devoted to learning language basics for the specific HDL being covered, including beginning circuit design.

The second day of the course focuses on the use of the HDL for circuit design, and synthesis-specific issues related to the use of HDLs for design. (One section is called Tricks and Traps, and helps the user to focus on understading what will result from synthesizing various HDL constructs.) More advanced topics, such as the use of hierarchy and timing analysis (and constraints) are also covered. Differences between simulatable and synthesizable HDL code are discussed. The high-level design methodology is discussed in more detail.

Tool

The software used is Exemplar's Leonardo synthesis software. Leonardo is an interactive, vendor-independent FPGA and ASIC synthesis tool that uses architecuture-specific synthesis algorithms to permit designers to fully utilize the target devices.